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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,872	09/29/2003	Douglas Fast	85195-102 ADB	8301

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EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2611 .	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,872	FAST ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/29/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 29 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-3 are objected to because of the following informalities:

a. In claim 1, lines 7-8, "phase locked loop" is suggested to be changed to "phase locked loop (PLL)".

b. In claim 1, line 13, the colon is suggested to be deleted.

c. In claim 2, line 21, "Context memory" is suggested to be changed to "context memory".

d. In claim 2, line 22 and claim 3, lines 4-5 and 6-7, "Voltage Controlled Oscillator" is suggested to be changed to "voltage controlled oscillator".

e. In claim 3, lines 3 and 6, "Phase Locked Loop" is suggested to be changed to "phase locked loop".

f. In claim 3, line 7, "Context" is suggested to be changed to "context".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites the limitation "A method of simultaneously synchronizing multiple input to multiple output signals", but does define when or how the signals are simultaneously synchronized. Without the clarification as to when or how the signals are synchronized though the limitations of the claims, one of ordinary skill in the art could not make/use the invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pinto et al. (U. S. Patent No. 5, 933, 058) in view of Yamashita (JP 11-220389A).

Regarding claim 1, Pinto et al. discloses a method of simultaneously synchronizing multiple extracted input clock signals to multiple output clock signals (as described in column 1, lines 8-19) using a self-tuning phase-locked loop (see Fig. 1, element 100), comprising:

communicating a plurality of signal pairs each comprising a clock input signal and an audio signal input (see Fig. 15, and column 16, lines 15-19), wherein the clock signal is extracted from the pair (as described in column 16, lines 15-19);

providing a discrete-time phase detector (see Fig. 1, block 102), loop filter (see Fig. 1, block 104), and voltage controlled oscillator (see Fig. 1, block 105) that together operate as a single discrete-time phase locked loop (see column 5, lines 5-19) in hardware for calculating an output signal (CLK(F0)) from an input signal (CLK(FD)) as shown in Fig. 1;

providing a PLL tuning logic (see Fig. 1, block 120) representing a control logic; and

providing a register (see Fig. 3, block 1051) representing a context memory for storing a frequency offset parameter for the clock signal (see column 6, lines 15-26) representing a history for the respective signal pair.

Pinto et al. does not disclose upon receipt at the discrete-time phase detector of the clock signal of a respective one of the signal pairs, operating the control (tuning) logic to retrieve from the context memory the history for the respective signal pair, to enable the discrete-time phase locked loop to calculate from the respective input signal a respective output signal thus defining a resulting history for the respective input signal, and to store the resulting history in the context memory for use in subsequent calculations for the respective input signal pair.

However, Yamashita discloses a phase locked loop circuit (see Fig. 1), which contains a control logic (see Fig. 1, block 3) for storing past variables for each clock cycle of the voltage controlled oscillator (see section 0008). The variable is representative of the previous phase comparisons (contrast) of the signal (clock) (see section 0008). Yamashita further discloses upon reception of a signal (clock), a phase contrast output by the phase comparator (see Fig. 1, block 1) is provided to the controller (see section 0027), wherein the controller reads hysteretic information stored in memory pertaining to the phase contrast (see section 0027). A controlled variable is then calculated from the hysteric information (see section 0008) and then stored in the

memory (see section 0028) to be used as a next controlled variable in subsequent calculations. The controlled variable is used to control a voltage controlled oscillator to provide an output signal (see sections 0028-0029). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use hysteric information to control the phase locked loop of Pinto et al. as disclosed by Yamashita since Yamashita discloses using hysteric information provides a low-cost and low power phase locked loop (see section 0033).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pinto et al. (U. S. Patent No. 5, 933, 058) in view of Yamashita (JP411220389A) as applied to claim 1, and in further view of Rozanski, Jr. et al. (U. S. Patent No. 4, 703, 520).

Regarding claim 2, Yamashita further discloses the memory is arranged to store and retrieve hysteric information for controlled variables which control a voltage controlled oscillator (see sections 0008 and 0028). It would have been obvious to include this feature since Yamashita discloses using hysteric information provides a low-cost and low power phase locked loop (see section 0033). However, Pinto et al. and Yamashita do not disclose the memory is arranged to store and retrieve history from the loop filter.

However, Rozanski, Jr. et al. discloses a phase locked loop which comprises of routing an output of a loop filter to memory to compare the current loop filter output with historical readings of the loop filter output (see column 2, lines 8-21). Further, in light of the comparison, the stored output can be provided to an oscillator instead of the current output (see column 2, lines 47-52). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to also store and retrieve information from the loop filter to control the phase detector of Pinto et al. and Yamashita as disclosed by Rozanski, Jr. et al. since Rozanski,

Jr et al. states using stored information maintains accurate frequency in the phase locked loop since aberrations that might ordinarily arise due to age or temperature are compensated (see column 2, lines 26-38).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pinto et al. (U. S. Patent No. 5, 933, 058) in view of Yamashita (JP 11-220389A) as applied to claim 1, and in further view of Wesolowski (US 2001/0015678).

Regarding claim 3, Pinto et al. further discloses the phase locked loop operates with system clock signals of different frequencies (see column 1, lines 59-63), wherein the tuning (control) logic (see Fig. 1, block 120) receives the system clock signals (see column 3, lines 53-55). Pinto et al. also discloses the tuning logic controls data reading modes (see column 13, lines 51-64) and writing to register memories (see column 14, lines 16-26). The tuning logic also provides a control signal (PFD_EN) to provide activation/deactivation (triggering) of the phase detector (see column 6, lines 5-11). Yamashita also further discloses a controller for storing (writing) and retrieving hysteric information for controlled variables which control a voltage controlled oscillator in a phase locked loop (see sections 0008 and 0028). It would have been obvious to include this feature since Yamashita discloses using hysteric information provides a low-cost and low power phase locked loop (see section 0033). However, Pinto et al. and Yamashita do not disclose storing (writing) and retrieving history of the loop filter and controlling routing of the input and output signals of the phase-locked loop.

However, Wesolowski discloses a phase locked loop (see Fig. 1), which includes a function control block (see Fig. 1, block 24), which controls the routing of input reference clock signals to the phase detector of the phase locked loop though element 28 of Fig. 1, (see also

section 0038) and routing of signals output from the filter of the phase detector through switch 34 of Fig. 1 (see section 0043 and 0050). The function control also controls the parameters of the PLL filter (see Fig. 1, block 32, section 0042) and the storage of the output control signal of the PLL filter which is retrieved for later use (see sections 0048-0049). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the control logic of Pinto et al. and Yamashita with the control functions of Wesolowski since Wesolowski states the function control block can shorten the phase lock acquisition time (see section 0042).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
October 24, 2006